

## CLAIMS

- 1 1. A method comprising:  
2 detecting a condition of an integrated circuit having a TAP while  
3 communicating with the TAP using a first TAP control device;  
4 and  
5 communicating with the TAP using a second TAP control device in  
6 response to detecting the condition.
- 1 2. The method of claim 1, wherein communicating with the TAP using a  
2 second TAP control device occurs in response to detecting the condition and  
3 issuing a second control signal to the second TAP control device.
- 1 3. The method of claim 1, wherein the condition is a failure of the  
2 integrated circuit.
- 1 4. The method of claim 1:  
2 wherein the condition is associated with a set of state data in the  
3 integrated circuit; and  
4 wherein communicating with the TAP using a second TAP control device,  
5 comprises reading the set of state data using the second TAP control device.
- 1 5. The method of claim 1, further comprising:  
2 maintaining the integrated circuit in the detected condition; and  
3 coupling the second TAP control device to the TAP while maintaining  
4 the integrated circuit in the detected condition.
- 1 6. The method of claim 5, wherein coupling the second TAP control device  
2 to the TAP occurs in response to a first control signal from the first TAP  
3 control device.

1 7. A method comprising:  
2 inputting test data from a first memory device to a test-access port of an  
3 integrated circuit; and  
4 storing state data associated with the input test data and output from the test-  
5 access port in a second memory device have a lower nominal speed rating than  
6 the first memory device.

1 8. The method of claim 7, wherein the first memory device stores vector  
2 test-pattern data and second memory device does not store.

1 9. The method of claim 7, wherein storing state data associated with the  
2 input test data occurs after:  
3 detecting existence of a desired condition of the integrated circuit; and  
4 decoupling the first memory device from at least a portion of the test  
5 access port.

1 10. A system comprising:  
2 first means for communicating with a test-access port of an integrated  
3 circuit;  
4 second means for communicating with a test-access port of an integrated  
5 circuit; and  
6 a multiplexer module, coupled between the test-access port and the first  
7 means and between the test-access port and the second means,  
8 for selectively coupling the first or second means to the test-  
9 access port.

1 11. The system of claim 10:  
2 wherein the first and second means include respective first and second  
3 sets of signal nodes for outputting or receiving signals from a  
4 test-access port; and

5 wherein the multiplexer module includes first and second multiplexers,  
6 with each multiplexer having a first input node coupled to one of  
7 the signal nodes in the first set of signal nodes and a second input  
8 node coupled to one of the signal nodes in the second set of  
9 signal nodes.

1 12. The system of claim 10, further comprising means for communicating a  
2 control signal from the first means to the second means to coordinate control of  
3 the test-access port.

1 13. The system of claim 10, wherein the first and second sets of signal  
2 nodes output or receive respective sets of JTAG signals.

1 14. Apparatus comprising:  
2 a first TAP control device having a first node for connection to a test  
3 port of an integrated circuit; and  
4 a multiplexer including first and second selectable nodes and a non-  
5 selectable node, with the first selectable node coupled to the first  
6 node of the first TAP control device and the non-selectable node  
7 for connection to the test port.

1 15. The apparatus of claim 14, further comprising a second TAP control  
2 device having a second node coupled to the second selectable node of  
3 the multiplexer.

1 16. The apparatus of claim 14, further comprising a vector pattern memory  
2 or algorithmic pattern generator coupled to the first TAP control device.

1 17. The apparatus of claim 14, wherein the first TAP control device  
2 comprises a JTAG boundary-scan controller.

1 18. Apparatus for selecting control of a test-access port of an integrated  
2 circuit, comprising:  
3 first means for electrical connection to a node of a first TAP control  
4 device;  
5 second means for electrical connection to a node of a second TAP  
6 control device;  
7 third means for electrical connection to a node of a test-access-port of  
8 an integrated circuit; and  
9 a first multiplexer coupled to the first, second, and third conductive  
10 means for selectively coupling the first or second means to the  
11 third means for electrical connection.

1 19. The apparatus of claim 18, further comprising a circuit board supporting  
2 the first multiplexer and the first, second, and third means.

1 20. The apparatus of claim 18, wherein the third means is for connection to  
2 one of a test clock node, a test-data-input node, a test-mode-select node, and a  
3 test-data-out node of the test-access port.

1 21. The apparatus of claim 18, further comprising:  
2 fourth means for connection to a node of the first TAP control device;  
3 fifth means for connection to a node of the second TAP control device;  
4 sixth means for connection to a node of the test-access-port; and  
5 a second multiplexer coupled to the fourth, fifth, and sixth conductive  
6 means for selectively coupling the fourth or fifth conductive  
7 means to the sixth conductive means.

1 22. Apparatus comprising:  
2 a first connector for connection to a first TAP control device;

3 a second connector for connection to a second TAP control device;  
4 a third connector for connection to a test-access-port of an integrated  
5 circuit; and  
6 a first multiplexer coupled to respective first, second, and third nodes of  
7 the first, second, and third connectors for selectively coupling the  
8 first or second nodes to the third nodes.

1 23. The apparatus of claim 22, further comprising a circuit board supporting  
2 the first multiplexer and the first, second, and third connectors.

1 24. The apparatus of claim 22, wherein each of the first, second, and third  
2 connectors includes a test clock node, a test-data-input node, a test-mode-select  
3 node, and a test-data-out node.

1 25. A machine-readable medium including coded instructions for operating  
2 a switching device to couple one of a plurality of TAP controllers to a TAP in  
3 an integrated circuit.

1 26. The machine-readable medium of claim 25, further including coded  
2 instructions for operating a device to detect a condition of the integrated circuit  
3 while using a first TAP controller and for communicating with the TAP using a  
4 second TAP control device in response to detection of the condition.

1 27. The medium of claim 25, wherein the condition is a failure of the  
2 integrated circuit.

1 28. The medium of claim 25, wherein the medium comprises an electronic,  
2 optical, or magnetic memory.